Patent claims

1. Method for fabricating a spacer structure, comprising the steps of:

a) forming a gate insulation layer (2) having a gate deposition-inhibiting layer (2A), a gate layer (3) and a covering deposition-inhibiting layer (4) on a semiconductor substrate (1);

b) patterning the gate layer (3) and the covering deposition-inhibiting layer (4) in order to form gate stacks (G); and

c) depositing an insulation layer (6) selectively with respect to the deposition-inhibiting layers (2A, 4) to form the spacer structure.

2. Method according to Patent Claim 1, characterized by the further step of

d) carrying out an implantation (I1) in order to form connection doping regions (LDD) in the semiconductor substrate (1).

3. Method according to one of Patent Claims 1 and 2, characterized by the further step of

e) depositing a further insulation layer (7) selectively with respect to the deposition-inhibiting layers (2A, 4) in order to form a widened spacer structure.

4. Method according to Patent Claim 3, characterized by the further step of

f) carrying out a further implantation (I2) in order to form source/drain regions (S/D) in the semiconductor substrate (1).

5. Method according to one of Patent Claims 1 to 4, characterized in that the deposition-inhibiting layers (2A, 4) include nitride layers and/or oxynitride layers

with a high nitrogen content, and ozone-enhanced TEOS deposition is carried out in step c) and/or step e).

6. Method according to one of Patent Claims 1 to 5, characterized in that the selectively deposited insulation layers (6, 7) at the side walls of the gate stack (G) have spacer layers (S6, S7) and at the deposition-inhibiting layers (2A, 4) have thin residual layers, the residual layers being removed by wet etching in a further step.

7. Method according to one of Patent Claims 1 to 6, characterized by the further step c1) and/or step e1) of densifying the selectively deposited insulation layers (6, 7).

8. Method according to one of Patent Claims 1 to 7, characterized by the further steps of
g) removing the deposition-inhibiting layers (2A, 4) in order to uncover the gate layer (3) and the semiconductor substrate (1);
h) depositing a material which can be silicided; and
i) converting a surface layer of the uncovered semiconductor substrate (1) and the gate layer (3) using the material which can be silicided in order to form highly conductive connection regions (8) for the source/drain regions (S/D) and the gate layer (3).

9. Method according to one of Patent Claims 1 to 8, characterized in that the gate layer (3) includes polycrystalline silicon and the semiconductor substrate (1) includes crystalline silicon.

10. Method according to one of Patent Claims 1 to 9, characterized in that it is used to fabricate field-effect transistors in the sub-100 nanometre range.